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CMOS Front-End Circuits of Dual-Band GPS Receiver

Yoshihiro UTSUROGI[†a)], *Nonmember*, Masaki HARUOKA[†,††], Toshimasa MATSUOKA[†],
and Kenji TANIGUCHI[†], *Members*

SUMMARY   A RF front-end chip for a dual-band Global Positioning System (GPS) receiver for L1 and L2 bands is designed using 0.25 μm CMOS technology. All function blocks of the GPS front-end are integrated onto one chip. The low noise amplifier has input matching over a wide frequency range to handle the L1 and L2 bands. This receiver uses a dual-band image-reject mixer with the quadrature mixer sharing a transconductor stage. This configuration enables the RF blocks to be shared with the L1 and L2 bands. The receiver has a chip area of 3.16 mm × 3.16 mm, and consumes 35 mA at 2.5 V.
key words: *dual-band GPS receiver, L1/L2, LNA, image-reject mixer, image-rejection ratio (IMRR)*

1.   Introduction

The Global Positioning System (GPS) has been widely used for applications which require position information such as car navigation systems and cellular phones. Although it was originally only a satellite-based survey system of global time based on atomic clocks, it is becoming important as an infrastructure which offers globally precise positioning and time information. A GPS satellite sends RF signals in two frequency bands, the L1 and L2 bands. The L1 (1.58 GHz) band carries the P code, which is limited to military use, together with the civil C/A-code, while the L2 (1.23 GHz) band is for military use only. However, launch of a satellite that will provide the C/A code for both the L1 and L2 bands is scheduled in the near future. Such a policy of GPS modernization gives rise to a new demand for simultaneous L1/L2 dual-band receivability, which can realize more precise positioning.

To meet such demand, we designed the front-end circuits of a dual-band GPS receiver using 0.25 μm CMOS technology, which can receive the L1 and L2 bands simultaneously. The receiver uses a dual-band image-reject mixer based on the Hartley architecture [1], which can handle two frequency bands and outputs each demodulated signal. The designed receiver shares a quadrature mixer for down-conversion of L1 and L2 signals, which is useful for reduction of power consumption and occupied area.

2.   Receiver Architecture

Figure 1 shows the block diagram of the designed front-end chip of the L1/L2 dual-band GPS receiver. All functional blocks for the GPS front-end circuits are integrated onto one chip. The down-converter is a double conversion system, consisting of a low noise amplifier (LNA), a Hartley-type image-reject mixer, a second mixer, and IF blocks including a variable gain amplifier (VGA), a Gm-C low-pass filter and a two-bit A/D converter. We used identical IF blocks for the L1 and L2 channels. The PLL synthesizer consists of a quadrature voltage-controlled oscillator (Q-VCO), frequency dividers, a phase frequency detector (PFD), a charge pump (CP), and a off-chip PLL loop filter.

The L1/L2 GPS signals from the external antenna are fed into the LNA, which handles the dual-band as described in Sect. 2.1. The first LO frequency is assigned to a position near the middle of the L1 and L2 bands, so that each of the bands becomes a complementary image of the other band. Thus, the image-reject (IR) mixer down-converts the L1/L2 signals to the first IF frequency signals [2]–[4]. The analog adder and subtracter in the IR mixer separate the L1/L2 signals. The IR mixer has a high image rejection ratio (IMRR), even without an external image-reject filter. The amplitude error of the first LO signals primarily deteriorates the IMRR in this architecture. Note that the Weaver architecture used in our previous works [2], [3] has additional IMRR deterioration caused by phase error in the second LO signals.

Moreover, the second mixer down-converts each of the separated signals to a second IF signal. The VGA in the IF blocks adjusts the voltage swing within a given range through the external auto gain control (AGC) loop, and the subsequent Gm-C low-pass filter eliminates out-of-band signals from the IF signal to avoid the occurrence of aliasing.

As shown in Fig. 1, this architecture can realize a dual-band GPS receiver with both low power consumption and small occupied area, because of the use of a shared quadrature mixer for down-conversion of L1 and L2 signals.

The first and second LO frequencies are 1391 MHz and 174 MHz, respectively. In this frequency plan, the second IF frequency for the L1/L2 signals is 10.23 MHz. Such high a second IF frequency is suitable for both C/A and P codes, although only C/A code main lobe is of concern in consumer low-power GPS CMOS receivers [5], [6]. This is another promising feature for the wide application of this front-end
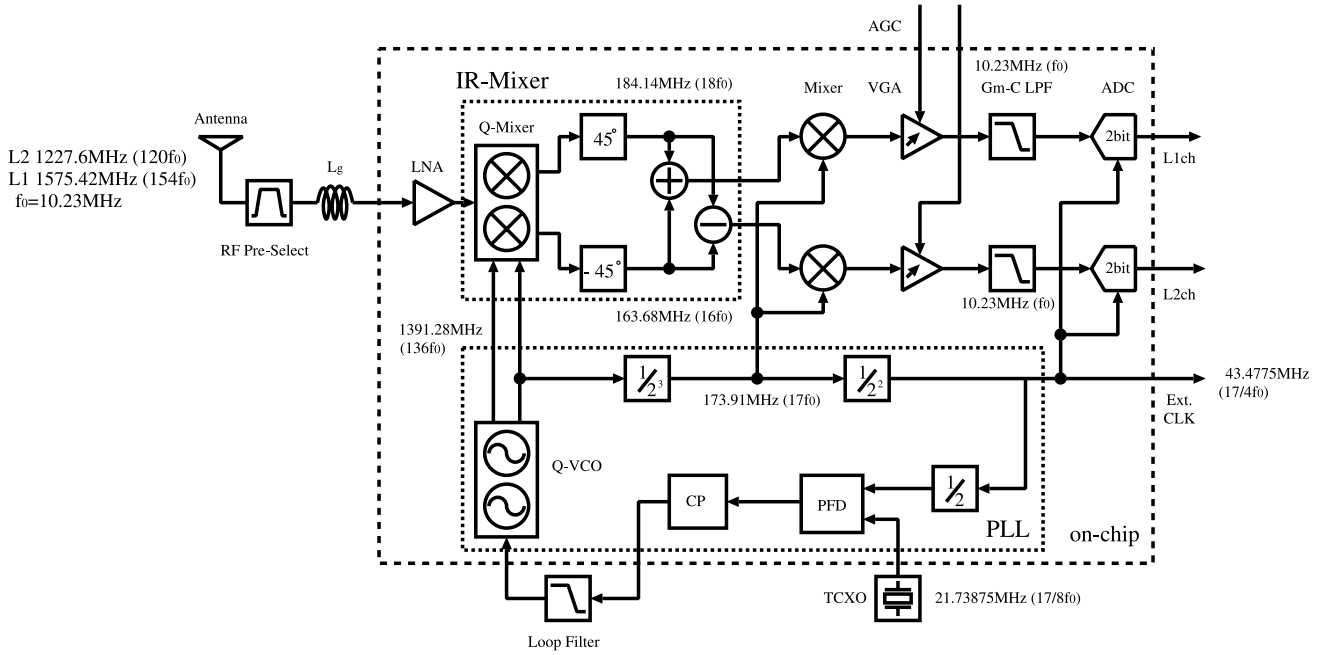
Fig. 1 Block diagram of dual-band GPS receiver (f_0: standard frequency of atomic clock in GPS satellite).

chip. The two-bit A/D converters sample the second IF signals at the rate of 43.4 MHz, which is greater than twice the upper bound of the second IF band (20.46 MHz).

2.1 LNA

Dual-band capability can be realized using an off-chip passive input matching network [7]. However, the L1/L2 dual-band LNA does not necessarily require this technique, because the desired signals are relatively close in frequency, which is useful for reducing the number of passive components.

Figure 2 shows the LNA used for the dual-band GPS receiver, which is based on an inductively degenerated common-source amplifier. The input impedance Z_{in} of the LNA is given by

$$Z_{in} = \frac{g_{m1}}{C_{gs}} L_s + j \left[\omega \left(L_s + L_g \right) - \frac{1}{\omega C_{gs}} \right], \qquad (1)$$

where g_{m1} and C_{gs} are the transconductance and the gate-source capacitance of the transistor M_1, respectively. Since the input reactance becomes zero at $\omega_0 = 1/\sqrt{C_{gs}(L_s + L_g)}$, the resistance at ω_0 must equal R_s for input impedance matching. The input Q factor is given by the following equation.

$$Q_{in} = \frac{1}{\omega_0 R_s C_{gs}} \qquad (2)$$

The magnitude of the input reflection coefficient $|S_{11}|$ is derived from Eqs. (1) and (2) as follows.

$$|S_{11}| = \left| \frac{jQ_{in} \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right)}{2 + jQ_{in} \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right)} \right| \qquad (3)$$
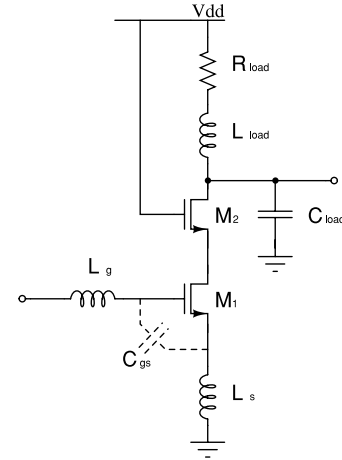

Fig. 2 Circuit of LNA.

Q_{in} must satisfy the following condition to keep $|S_{11}|$ below Γ [dB] in the frequency range from the L1 band to the L2 band.

$$Q_{in} < \frac{2 \times 10^{\frac{\Gamma}{20}}}{\sqrt{1 - 10^{\frac{\Gamma}{10}} \cdot \left| \frac{\omega_{1,2}}{\omega_0} - \frac{\omega_0}{\omega_{1,2}} \right|}} \qquad (4)$$

Here, $\omega_{1,2}$ is the frequency of the L1 and L2 bands, and ω_0 is their geometric mean. Figure 3 shows the NF calculated with the following relation [8].

$$NF \approx 1 + \frac{\gamma}{\alpha} \frac{\chi}{Q_{in}} \left(\frac{\omega_0}{\omega_T} \right), \qquad (5)$$

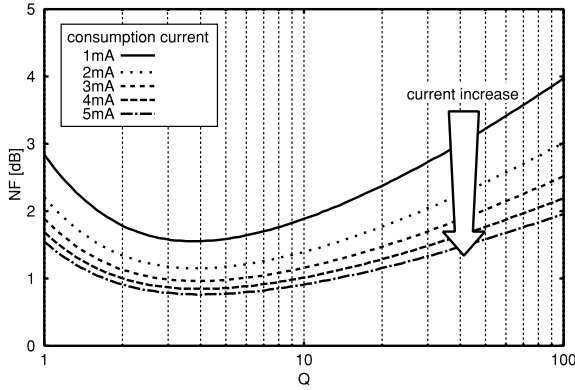$$\chi = 1 + 2|c| \sqrt{\frac{\delta \alpha^2}{\kappa \gamma}} + \frac{\delta \alpha^2}{\kappa \gamma} \left(1 + Q_{in}^2 \right) \qquad (6)$$

Fig. 3 Analytical calculation of *NF* versus Q_{in} in LNA as a function of current consumption.
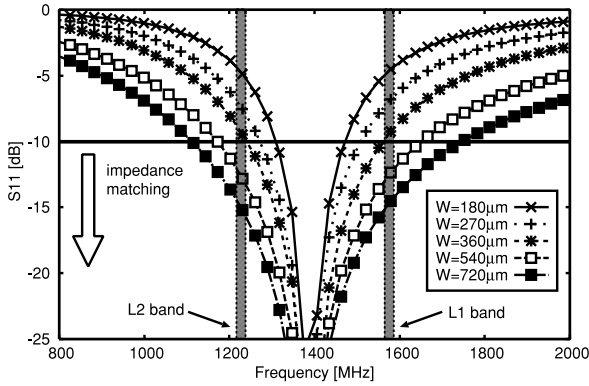

Fig. 4 Simulated S11 of LNA.

The Q_{in} of the dual-band LNA must be chosen so as to minimize *NF* under the constraint given by Eq. (4). Eq. (2) suggests that an increase in C_{gs} leads to a low Q_{in}, resulting in impedance matching over a wide frequency range [9]. Figure 4 shows the calculated $|S_{11}|$ as a function of the gate width *W* of M_1 under the L1/L2 geometric mean f_0 of 1391 MHz. It turns out that a value of *W* over 540 μm results in $|S_{11}| < -10$ dB in the frequency range from the L1 band to the L2 band. Thus, both low *NF* and dual-band capability are realized under the condition of input impedance matching. In addition, the quality factor of the load tank circuit is reduced by placing R_{load} in series with L_{load} as shown in Fig. 2.

2.2 Image-Reject Mixer and VCO

The Hartley-type image-reject mixer shown in Fig. 5 consists of a quadrature mixer and two poly phase filters [10] for L1 and L2 channels. The poly phase filter acts as either an adder or a subtracter depending on the phase of the input signal. As shown in Fig. 5, the I-phase of L1 inputs in poly phase filters is in phase with that of the L2 channel, while the Q-phase inputs have the opposite phase to derive the L1 and L2 channels. In the output stage, for example, the desired and the image signals in the L1 channel are L1 and L2 signals, respectively. The IMRR is limited by the
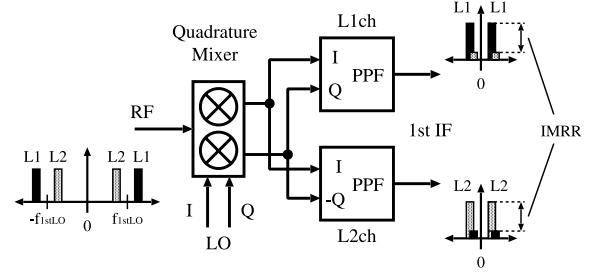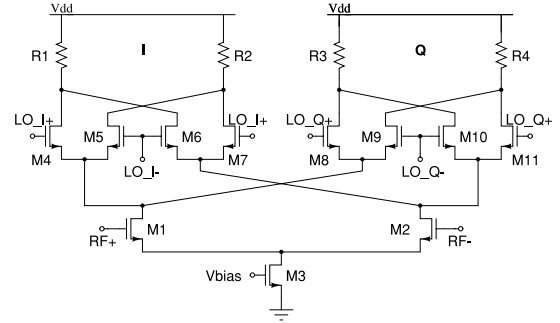

Fig. 5 Block diagram of image-reject mixer.

Fig. 6 Quadrature mixer with shared transconductor.
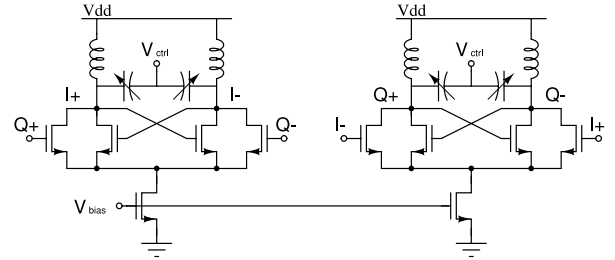

Fig. 7 Quadrature-coupled LC-VCO.

mismatch of the quadrature mixer, polyphase filter, and IQ accuracy of the LO signal.

Figure 6 shows the quadrature mixer with a shared transconductor for the I and Q phases [2], [3], [11]–[13]. Both the conversion gain and noise figure are improved by 3 dB at a given bias current due to the different switching characteristic compared with a conventional Gilbert mixer. Moreover, the quadrature mixer compensates the phase error of LO.

Figure 7 shows a quadrature-coupled-type LC VCO (Q-VCO) [14]–[17] for generating IQ LO signals. Although mismatch in physical layout and process variation in the load impedance deteriorates the IQ accuracy of the Q-VCO, the circuit simulation proves that an IMRR of over 30 dB is achievable even in the case of 5% mismatch of capacitances in the tank circuit at the output terminals.

2.3 IF Blocks

A VGA composed of two-stage differential amplifiers is used to achieve gain control in the range over 60 dB, which compensates for temperature and process variations in the receiver. A second-order Gm-C low-pass filter [18] is used for band limitation of the second IF. In this design, the bias current of the transconductor is controlled using the band gap reference circuit, which reduces the temperature dependence of the transconductance. The circuit simulation confirmed that variation of the cut-off frequency is reduced within 1.2% over the temperature range of −45–85℃, while the influence of process variation is approximately 9%.

3. Experimental Results

The front-end chip of a dual-band GPS receiver was fabricated using 0.25 μm CMOS technology. A photograph of the chip is shown in Fig. 8. The chip area is 3.16 mm × 3.16 mm, and current consumption is 35 mA at 2.5 V. Figure 9 shows a printed circuit board using a 52-pin LCC package that was used to measure the RF characteristics of the chip.

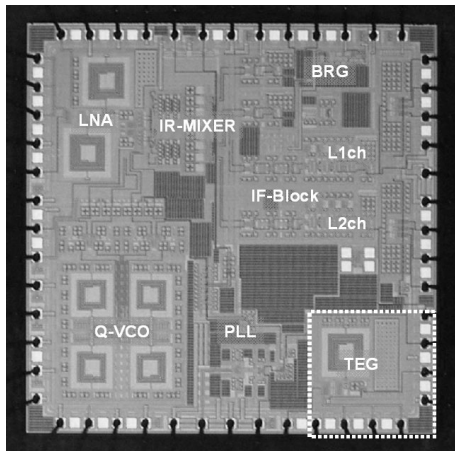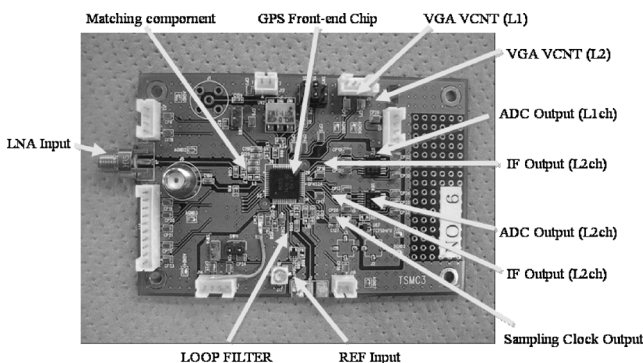The measured S_{11} of LNA with an off-chip surface-mount-type inductor for input impedance matching is shown in Fig. 10. The return loss less than −10 dB is achieved in the L1/L2 frequency range. The LNA has a voltage gain of 25 dB for both L1 and L2 bands with a current of 5 mA. The noise figures are 4.0 dB and 5.8 dB for the L1 and L2 bands, respectively.

Figure 11 shows the second IF signal spectrum at the output terminal (L1ch) of the Gm-C low-pass-filter. The RF carrier signal (L1:1575.42 MHz) fed into the dual-band GPS front-end chip is down-converted to 10.23 MHz, where the A/D converter is turned off. The dominant spurious level is less than −25 dBc. Moreover, the noise floor observed in the figure reflects the frequency characteristic of receiver gain.

Figure 12 shows the blocking characteristics of the front-end chip at the receiver gain of 68.5 dB without an external filter. The blocking level is measured by evaluating the power of the interference CW signal which decreases the desired signal level by 1 dB at an RF input signal of −84 dBm. The blocking characteristics deteriorate for the blocker signal near 1900 MHz. This is attributed to the down-conversion of the third harmonics in the second LO signal to the second IF band. Figure 12 shows that the interference wave of the L1/L2 band does not affect either channel up to −40 dBm. This feature reflects the high IMRR (>
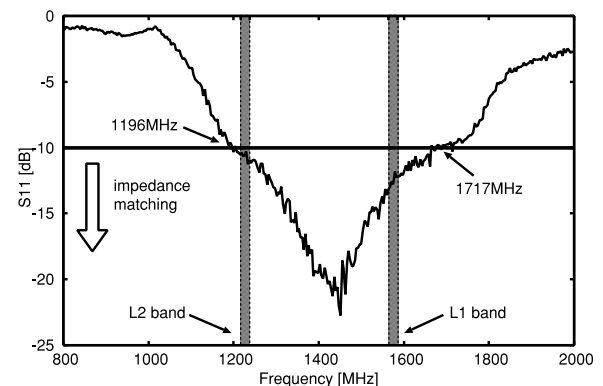

Fig. 8 Photograph of fabricated chip.

Fig. 9 Printed circuit board for evaluation.

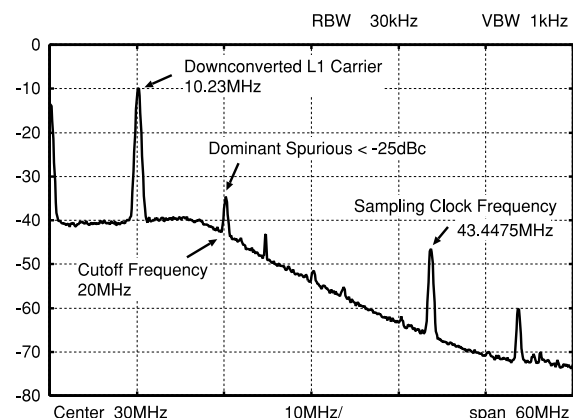**Fig. 10** Measured S11 of LNA.

Fig. 11 Spectrum of second IF signal at output terminal (L1ch) of Gm-C low-pass-filter.

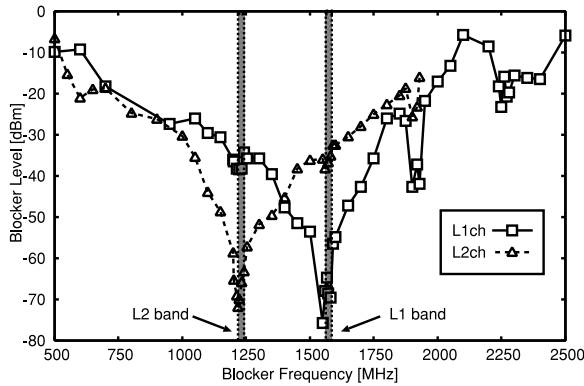**Fig. 12** 1 dB blocking point.

Table 1 Receiver performance summary.

Supply Voltage	2.5 V
Supply Current	35 mA
Maximum Gain	85 dB
VGA range	65 dB
Input S11	< -10 dB
NF_{DSB} (L1ch / L2ch)	7 dB / 8 dB
$P_{1 dB}$	-35 dB @ Min Gain
Image Rejection Ratio	32 dB
Filter Cutoff Frequency	20 MHz
Filter Stopband Attenuation	-30 dB @ 50 MHz
Spurious Level @ ADC OFF / ON	< -25 dBc / < -23 dBc
LO leakage to RF	-63 dBm
PLL In-band Phase Noise	< -77.7 dBc/Hz
PLL spurs	-58 dBc
1st LO Frequency	1391.28 MHz
2nd LO Frequency	173.91 MHz
Baseband Frequency	10.23 MHz
Sampling Clock Frequency	43.44775 MHz

30 dB).

The measured characteristics of the GPS receiver frontend chip are summarized in Table 1.

4. Conclusions

The front-end chip of a dual-band GPS receiver for the L1 and L2 bands is designed using 0.25 μm CMOS technology. The RF block is characterized with the first Hartley-type image-rejection mixer shared by the L1 and L2 channels. The proposed dual-band receiver shares a quadrature mixer for down-conversion of L1 and L2 signals, which is useful for reducing the power consumption and occupied area. The occupied area of the fabricated chip is 3.16 mm × 3.16 mm, and the current consumption is 35 mA at 2.5 V. The fabricated dual-band GPS front-end chip has a maximum voltage gain of 85 dB, a variable range of 65 dB, a NF of 8 dB, and a IMRR of 32 dB.

Acknowledgments

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